

## 240pin Unbuffered DDR2 SDRAM MODULE

Based on 128Mx8 DDR2 SDRAM D-die

### Features

Performance:

		PC2-8500	
Speed Sort		-BD	Unit
DIMM $\overline{\text{CAS}}$ Latency*		6	
f <sub>CK</sub>	Clock Frequency	533	MHz
t <sub>CK</sub>	Clock Cycle	1.875	ns
f <sub>DQ</sub>	DQ Burst Frequency	1066	Mbps

- 240-pin Dual In-Line Memory Module
- 128Mx64 and 256Mx64 DDR2 Unbuffered DIMM based on Elixir 128Mx8 DDR2 SDRAM D-die component
- Intended for 533 MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ} = 1.8V \pm 0.1V$
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - Device  $\overline{\text{CAS}}$  Latency: 4, 5, 6
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/1 Addressing (row/column/rank) – 1GB
- 14/10/2 Addressing (row/column/rank) – 2GB
- 7.8  $\mu\text{s}$  Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 60 ball BGA Package
- RoHS compliance

### Description

M2Y1G64TU88D4B, M2Y1G64TU88D5B, M2Y1G64TU88D6B, M2Y2G64TU8HD4B, M2Y2G64TU8HD5B, M2Y2G64TU8HD6B and M2Y1G64TU88D7B are 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as one rank 128Mx64 and two ranks 256Mx64 high-speed memory array. M2Y1G64TU88D4B, M2Y1G64TU88D5B, M2Y1G64TU88D6B and M2Y1G64TU88D7B use eight 128Mx8 DDR2 SDRAMs. M2Y2G64TU8HD4B, M2Y2G64TU8HD5B and M2Y2G64TU8HD6B use sixteen 128Mx8 DDR2 SDRAMs in BGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All Elixir DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 533MHz clock speeds and achieves high-speed data transfer rates of up to 1066Mbps. Prior to any access operation, the device  $\overline{\text{CAS}}$  latency and burst / length /operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0, BA1 and BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

## Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M2Y1G64TU88D4B-BD	533MHz (1.875ns @ CL = 6)	DDR2-1066	PC2-8500	128Mx64	GOLD	1.8V	
M2Y1G64TU88D5B-BD	533MHz (1.875ns @ CL = 6)	DDR2-1066	PC2-8500				
M2Y1G64TU88D6B-BD	533MHz (1.875ns @ CL = 6)	DDR2-1066	PC2-8500				
M2Y1G64TU88D7B-BD	533MHz (1.875ns @ CL = 6)	DDR2-1066	PC2-8500				
M2Y2G64TU8HD4B-BD	533MHz (1.875ns @ CL = 6)	DDR2-1066	PC2-8500	256Mx64			
M2Y2G64TU8HD5B-BD	533MHz (1.875ns @ CL = 6)	DDR2-1066	PC2-8500				
M2Y2G64TU8HD6B-BD	533MHz (1.875ns @ CL = 6)	DDR2-1066	PC2-8500				

## Pin Description

CK0~CK2 CK0~CK2	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS8	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	DM0-DM8	Input Data Mask
$\overline{CAS}$	Column Address Strobe	$\overline{DQS0-DQS8}$	Differential data strobes
$\overline{WE}$	Write Enable	VDD	Power (1.8V)
$\overline{CS0}$ , $\overline{CS1}$	Chip Selects	VREF	Ref. Voltage for SSTL_18 inputs
A0-A9, A0-A13	Address Inputs	VDDSPD	Serial EEPROM positive power supply
A10/AP	Column Address Input/Auto-precharge	VSS	Ground
BA0 ~ BA2	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RESET	Reset pin	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	On-die termination control lines	SA0 ~ SA2	Serial Presence Detect Address Inputs
NC	No Connect		

Note: ODT1, CKE1 and  $\overline{CS1}$  are only support in 2GB module type.

## Pinout

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V <sub>REF</sub>	42	NC	82	V <sub>SS</sub>	121	V <sub>SS</sub>	162	NC	202	DM4
2	V <sub>SS</sub>	43	NC	83	$\overline{DQS4}$	122	DQ4	163	V <sub>SS</sub>	203	NC
3	DQ0	44	V <sub>SS</sub>	84	DQS4	123	DQ5	164	NC	204	V <sub>SS</sub>
4	DQ1	45	NC <sup>-</sup>	85	V <sub>SS</sub>	124	V <sub>SS</sub>	165	NC	205	DQ38
5	V <sub>SS</sub>	46	NC	86	DQ34	125	DM0	166	V <sub>SS</sub>	206	DQ39
6	$\overline{DQS0}$	47	V <sub>SS</sub>	87	DQ35	126	NC	167	NC	207	V <sub>SS</sub>
7	DQS0	48	NC	88	V <sub>SS</sub>	127	V <sub>SS</sub>	168	NC	208	DQ44
8	V <sub>SS</sub>	49	NC	89	DQ40	128	DQ6	169	V <sub>SS</sub>	209	DQ45
9	DQ2	50	V <sub>SS</sub>	90	DQ41	129	DQ7	170	V <sub>DDQ</sub>	210	V <sub>SS</sub>
10	DQ3	51	V <sub>DDQ</sub>	91	V <sub>SS</sub>	130	V <sub>SS</sub>	171	NC,CKE1	211	DM5
11	V <sub>SS</sub>	52	CKE0	92	$\overline{DQS5}$	131	DQ12	172	V <sub>DD</sub>	212	NC
12	DQ8	53	V <sub>DD</sub>	93	DQS5	132	DQ13	173	NC	213	V <sub>SS</sub>
13	DQ9	54	BA2	94	V <sub>SS</sub>	133	V <sub>SS</sub>	174	NC	214	DQ46
14	V <sub>SS</sub>	55	NC	95	DQ42	134	DM1	175	V <sub>DDQ</sub>	215	DQ47
15	$\overline{DQS1}$	56	V <sub>DDQ</sub>	96	DQ43	135	NC	176	A12	216	V <sub>SS</sub>
16	DQS1	57	A11	97	V <sub>SS</sub>	136	V <sub>SS</sub>	177	A9	217	DQ52
17	V <sub>SS</sub>	58	A7	98	DQ48	137	CK1	178	V <sub>DD</sub>	218	DQ53
18	NC	59	V <sub>DD</sub>	99	DQ49	138	$\overline{CK1}$	179	A8	219	V <sub>SS</sub>
19	NC	60	A5	100	V <sub>SS</sub>	139	V <sub>SS</sub>	180	A6	220	CK2
20	V <sub>SS</sub>	61	A4	101	SA2	140	DQ14	181	V <sub>DDQ</sub>	221	$\overline{CK2}$
21	DQ10	62	V <sub>DDQ</sub>	102	NC	141	DQ15	182	A3	222	V <sub>SS</sub>
22	DQ11	63	A2	103	V <sub>SS</sub>	142	V <sub>SS</sub>	183	A1	223	DM6
23	V <sub>SS</sub>	64	V <sub>DD</sub>	104	$\overline{DQS6}$	143	DQ20	184	V <sub>DD</sub>	224	NC
24	DQ16	KEY		105	DQS6	144	DQ21	KEY		225	V <sub>SS</sub>
25	DQ17	65	V <sub>SS</sub>	106	V <sub>SS</sub>	145	V <sub>SS</sub>	185	CK0	226	DQ54
26	V <sub>SS</sub>	66	V <sub>SS</sub>	107	DQ50	146	DM2	186	$\overline{CK0}$	227	DQ55
27	$\overline{DQS2}$	67	V <sub>DD</sub>	108	DQ51	147	NC	187	V <sub>DD</sub>	228	V <sub>SS</sub>
28	DQS2	68	NC	109	V <sub>SS</sub>	148	V <sub>SS</sub>	188	A0	229	DQ60
29	V <sub>SS</sub>	69	V <sub>DD</sub>	110	DQ56	149	DQ22	189	V <sub>DD</sub>	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	V <sub>SS</sub>
31	DQ19	71	BA0	112	V <sub>SS</sub>	151	V <sub>SS</sub>	191	V <sub>DDQ</sub>	232	DM7
32	V <sub>SS</sub>	72	V <sub>DDQ</sub>	113	$\overline{DQS7}$	152	DQ28	192	$\overline{RAS}$	233	NC
33	DQ24	73	$\overline{WE}$	114	DQS7	153	DQ29	193	$\overline{CS0}$	234	V <sub>SS</sub>
34	DQ25	74	$\overline{CAS}$	115	V <sub>SS</sub>	154	V <sub>SS</sub>	194	V <sub>DDQ</sub>	235	DQ62
35	V <sub>SS</sub>	75	V <sub>DDQ</sub>	116	DQ58	155	DM3	195	ODT0	236	DQ63
36	$\overline{DQS3}$	76	$\overline{NC,CS1}$	117	DQ59	156	NC	196	A13	237	V <sub>SS</sub>
37	DQS3	77	NC,ODT1	118	V <sub>SS</sub>	157	V <sub>SS</sub>	197	V <sub>DD</sub>	238	V <sub>DDSPD</sub>
38	V <sub>SS</sub>	78	V <sub>DDQ</sub>	119	SDA	158	DQ30	198	V <sub>SS</sub>	239	SA0
39	DQ26	79	V <sub>SS</sub>	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	V <sub>SS</sub>	200	DQ37		
41	V <sub>SS</sub>	81	DQ33			161	NC	201	V <sub>SS</sub>		

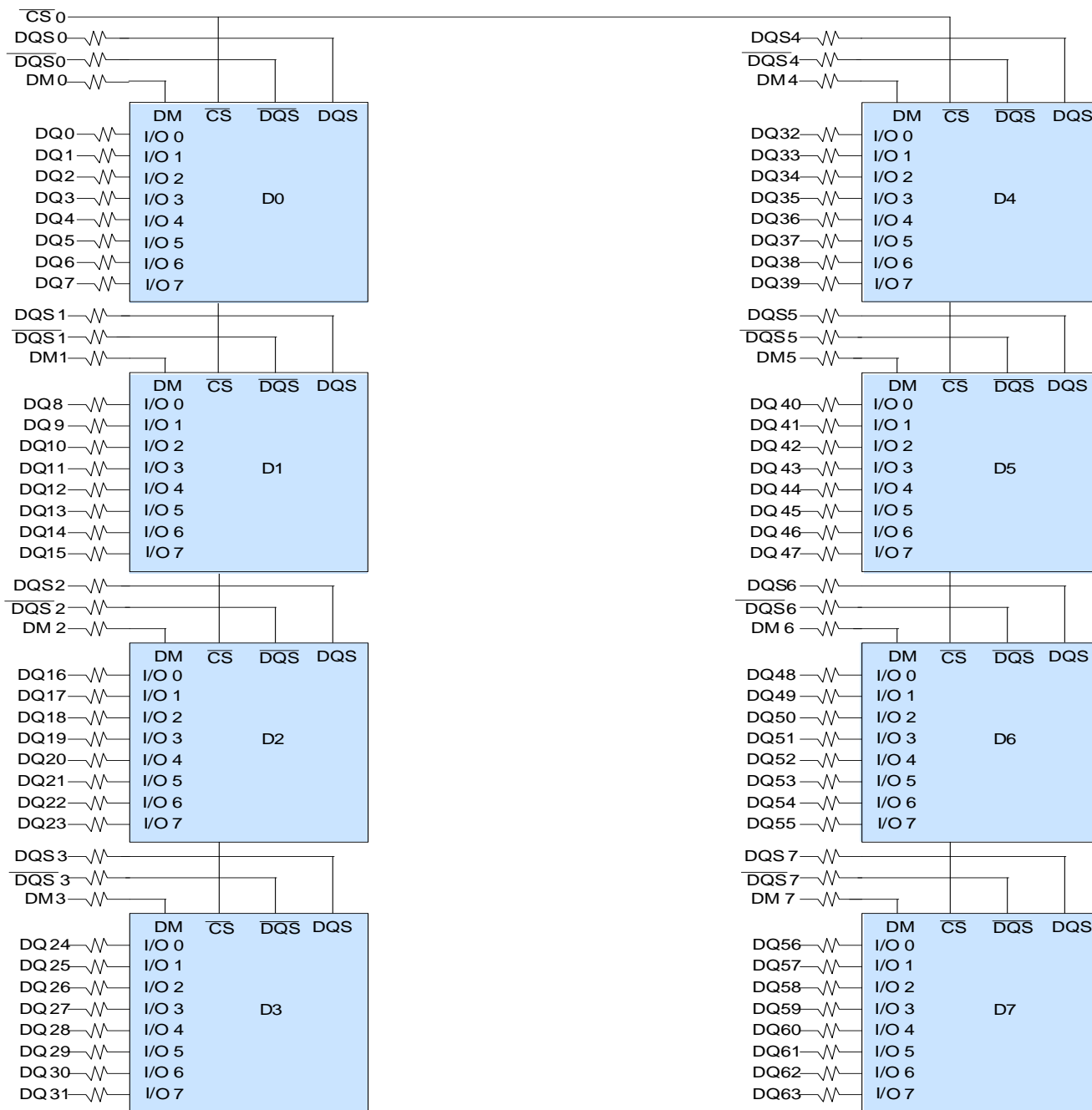
Note:

1. NC = No Connect.
2.  $\overline{CS1}$ , ODT1 and CKE1 (Pins 76, 77 and 171) are only support in 2GB module type.

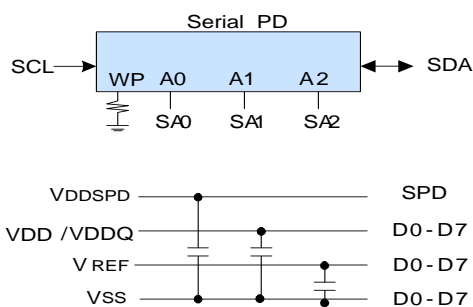
## Input/output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$ , $\overline{CK1}$ , $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode. CKE1 apply on 2GB UDIMM only.
$\overline{CS0}$ , $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. $\overline{CS1}$ apply on 2GB UDIMM only.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL-18 inputs
VDDQ	Supply		Isolated power supply for the DDR2 SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals. ODT1 apply on 2GB UDIMM only.
BA0 – BA2	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/output pins.
VDD, VSS	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic
DQS0 – DQS8 $\overline{DQS0}$ – $\overline{DQS8}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either VDD or VSS on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pull-up.
VDDSPD	Supply		Serial EEPROM positive power supply.

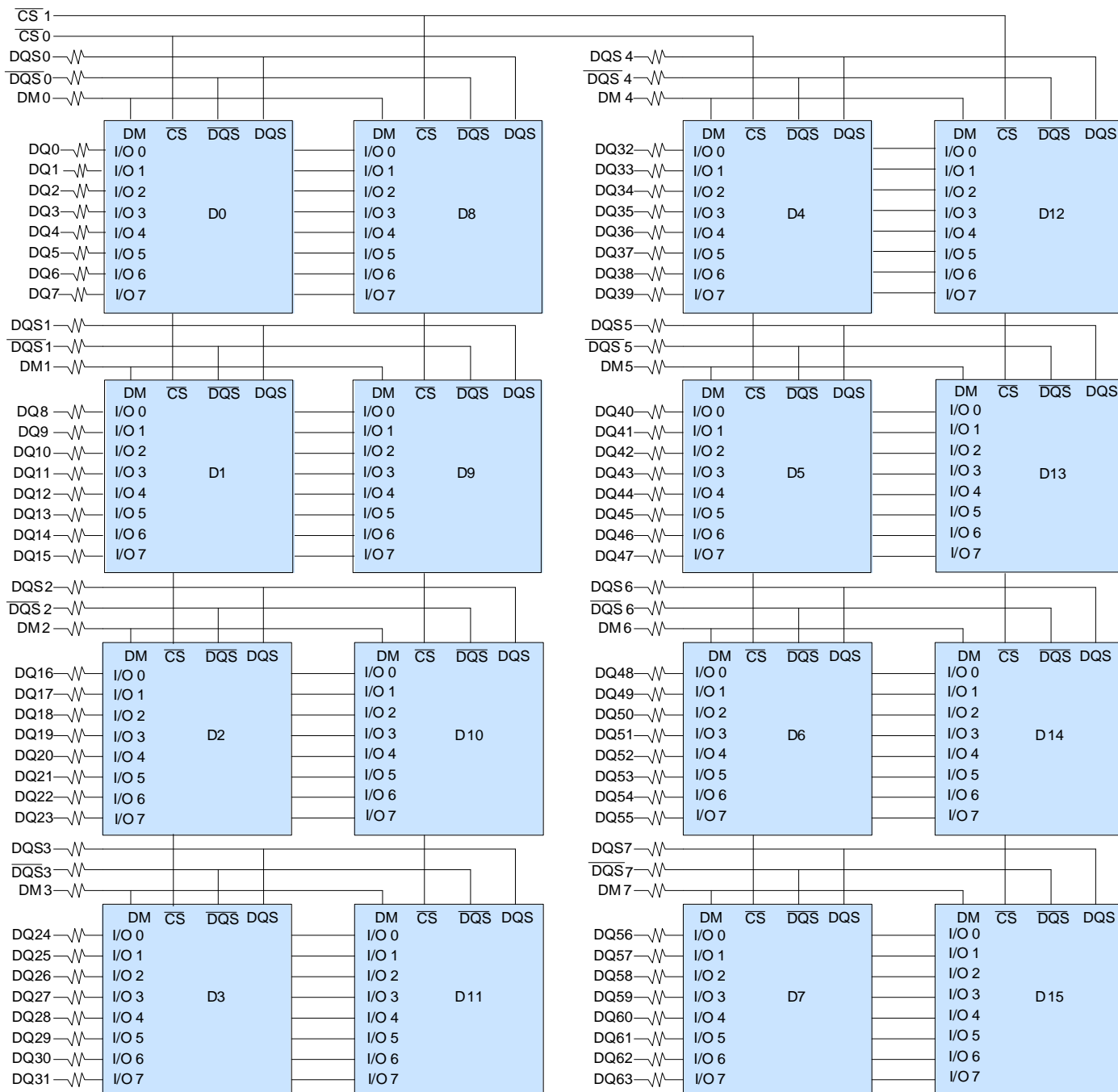
**Functional Block Diagram** (1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)



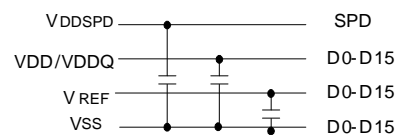
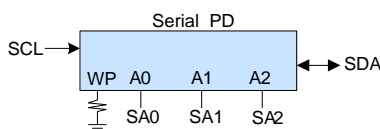
BA0-BA2 → BA0-BA2: SDRAMs D0-D7  
A0-A13 → A0-A13: SDRAMs D0-D7  
RAS → RAS: SDRAMs D0-D7  
CAS → CAS: SDRAMs D0-D7  
WE → WE: SDRAMs D0-D7  
CKE0 → CKE: SDRAMs D0-D7  
ODT0 → ODT: SDRAMs D0-D7



**Functional Block Diagram** (2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)



- BA0-BA2 → BA0 - BA2 : SDRAMs D0-D15
- A0-A13 → A0 - A13 : SDRAMs D0-D15
- RAS → RAS : SDRAMs D0-D15
- CAS → CAS : SDRAMs D0-D15
- WE → WE : SDRAMs D0-D15
- CKE0 → CKE : SDRAMs D0-D7
- CKE1 → CKE : SDRAMs D8-D15
- ODT0 → ODT : SDRAMs D0-D7
- ODT1 → ODT : SDRAMs D8-D15



## Serial Presence Detect -- Part 1 of 2 (1GB)

128Mx64 1RANK UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Note
		PC2-8500 -BD	PC2-8500 -BD	
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	DDR2	08	
3	Number of Row Addresses on Assembly	14	0E	
4	Number of Column Addresses on Assembly	10	0A	
5	Number of DIMM Ranks	1 rank, Height=30mm	60	
6	Data Width of Assembly	X64	40	
7	Reserved	Undefined	00	
8	Voltage Interface Level of this Assembly	SSTL_1.8V	05	
9	DDR2 SDRAM Device Cycle Time at CL=5	1.875ns	18	
10	DDR2 SDRAM Device Access Time from Clock at CL=5	0.35ns	35	
11	DIMM Configuration Type	Non parity/ECC	00	
12	Refresh Rate/Type	7.8µs	82	
13	Primary DDR2 SDRAM Width	X8	08	
14	Error Checking DDR2 SDRAM Device Width	Undefined	00	
15	Reserved	Undefined	00	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8	0C	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8	08	
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	4,5,6	70	
19	DIMM Mechanical Characteristics	x ≤ 4.10 (mm)	01	
20	DDR2 SDRAM DIMM Type Information	UDIMM (133.35mm)	02	
21	DDR2 SDRAM Module Attributes:	Normal DIMM	00	
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50Ω ODT, and PASR	07	
23	Minimum Clock Cycle at CL=4	2.5ns	25	
24	Maximum Data Access Time from Clock at CL=4	0.4ns	40	
25	Minimum Clock Cycle Time at CL=3	3ns	30	
26	Maximum Data Access Time from Clock at CL=3	0.45ns	45	
27	Minimum Row Precharge Time (t <sub>RP</sub> )	11.25ns	2D	
28	Minimum Row Active to Row Active delay (t <sub>RRD</sub> )	7.5ns	1E	
29	Minimum RAS to CAS delay (t <sub>RCD</sub> )	11.25ns	2D	
30	Minimum RAS Pulse Width (t <sub>RAS</sub> )	45ns	2D	
31	Module Bank Density	1GB	01	
32	Address and Command Setup Time Before Clock (t <sub>IS</sub> )	0.12ns	12	
33	Address and Command Hold Time After Clock (t <sub>IH</sub> )	0.20ns	20	
34	Data Input Setup Time Before Clock (t <sub>DS</sub> )	Undefined	00	
35	Data Input Hold Time After Clock (t <sub>DH</sub> )	0.07ns	07	
36	Write Recovery Time (t <sub>WR</sub> )	15.0ns	3C	
37	Internal Write to Read Command delay (t <sub>WTR</sub> )	7.5ns	1E	
38	Internal Read to Precharge delay (t <sub>RTP</sub> )	7.5ns	1E	
39	Reserved	Undefined	00	

## Serial Presence Detect -- Part 2 of 2 (1GB)

128Mx64 1RANK UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Note
		PC2-8500 -BD	PC2-8500 -BD	
40	Extension of Byte 41 $t_{RC}$ and Byte 42 $t_{RFC}$	The number below a decimal point of $t_{RC}$ and $t_{RFC}$ are 0, $t_{RFC}$ is less than 256ns.	16	
41	Minimum Core Cycle Time ( $t_{RC}$ )	56.25ns	38	
42	Min. Auto Refresh Command Cycle Time ( $t_{RFC}$ )	127.5ns	7F	
43	Maximum Clock Cycle Time ( $t_{CK}$ )	8.0ns	80	
44	Max. DQS-DQ Skew Factor ( $t_{DQS}$ )	0.17ns	11	
45	Read Data Hold Skew Factor ( $t_{QHS}$ )	0.25ns	19	
46	PLL Relock Time	Undefined	00	
46-61	Reserved	Undefined	00	
62	SPD Revision	1.3	13	
63	Checksum for bytes 0-62	Checksum Data	6D	
64-71	Manufacture's JEDEC ID Code	NANYA	7F7F7F0B00000000	
72	Module Manufacturing Location	Manufacturing Code	--	
73-91	Module Part number	Module Part Number in ASCII	--	1
92-255	Reserved	Undefined	--	

Note 1:  
M2Y1G64TU88D4B-BD → 4D325931473634545538384434422D42442020  
M2Y1G64TU88D5B-BD → 4D325931473634545538384435422D42442020  
M2Y1G64TU88D6B-BD → 4D325931473634545538384436422D42442020  
M2Y1G64TU88D7B-BD → 4D325931473634545538384437422D42442020

## Serial Presence Detect -- Part 1 of 2 (2GB)

256Mx64 2RANKs UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Note
		PC2-8500 -BD	PC2-8500 -BD	
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	DDR2	08	
3	Number of Row Addresses on Assembly	14	0E	
4	Number of Column Addresses on Assembly	10	0A	
5	Number of DIMM Ranks	2 ranks, Height=30mm	61	
6	Data Width of Assembly	X64	40	
7	Reserved	Undefined	00	
8	Voltage Interface Level of this Assembly	SSTL_1.8V	05	
9	DDR2 SDRAM Device Cycle Time at CL=5	1.875ns	18	
10	DDR2 SDRAM Device Access Time from Clock at CL=5	0.35ns	35	
11	DIMM Configuration Type	Non parity/ECC	00	
12	Refresh Rate/Type	7.8µs	82	
13	Primary DDR2 SDRAM Width	X8	08	
14	Error Checking DDR2 SDRAM Device Width	Undefined	00	
15	Reserved	Undefined	00	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8	0C	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8	08	
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	4,5,6	70	
19	DIMM Mechanical Characteristics	x ≤ 4.10 (mm)	01	
20	DDR2 SDRAM DIMM Type Information	UDIMM (133.35mm)	02	
21	DDR2 SDRAM Module Attributes:	Normal DIMM	00	
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50Ω ODT, and PASR	07	
23	Minimum Clock Cycle at CL=4	2.5ns	25	
24	Maximum Data Access Time from Clock at CL=4	0.4ns	40	
25	Minimum Clock Cycle Time at CL=3	3.0ns	30	
26	Maximum Data Access Time from Clock at CL=3	0.45ns	45	
27	Minimum Row Precharge Time (t <sub>RP</sub> )	11.25ns	2D	
28	Minimum Row Active to Row Active delay (t <sub>RRD</sub> )	7.5ns	1E	
29	Minimum RAS to CAS delay (t <sub>RCD</sub> )	11.25ns	2D	
30	Minimum RAS Pulse Width (t <sub>RAS</sub> )	45ns	2D	
31	Module Bank Density	1GB	01	
32	Address and Command Setup Time Before Clock (t <sub>IS</sub> )	0.12ns	12	
33	Address and Command Hold Time After Clock (t <sub>IH</sub> )	0.20ns	20	
34	Data Input Setup Time Before Clock (t <sub>DS</sub> )	Undefined	00	
35	Data Input Hold Time After Clock (t <sub>DH</sub> )	0.07ns	07	
36	Write Recovery Time (t <sub>WR</sub> )	15.0ns	3C	
37	Internal Write to Read Command delay (t <sub>WTR</sub> )	7.5ns	1E	
38	Internal Read to Precharge delay (t <sub>RTP</sub> )	7.5ns	1E	
39	Reserved	Undefined	00	

### Serial Presence Detect -- Part 2 of 2 (2GB)

256Mx64 2RANKs UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Note
		PC2-8500 -BD	PC2-8500 -BD	
40	Extension of Byte 41 tRC and Byte 42 tRFC	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.	16	
41	Minimum Core Cycle Time (tRC)	56.25ns	38	
42	Min. Auto Refresh Command Cycle Time (tRFC)	127.5ns	7F	
43	Maximum Clock Cycle Time (tCK)	8.0ns	80	
44	Max. DQS-DQ Skew Factor (tQHS)	0.17ns	11	
45	Read Data Hold Skew Factor (tQHS)	0.25ns	19	
46	PLL Relock Time	Undefined	00	
46-61	Reserved	Undefined	00	
62	SPD Revision	1.3	13	
63	Checksum for bytes 0-62	Checksum Data	6E	
64-71	Manufacture's JEDEC ID Code	NANYA	7F7F7F0B00000000	
72	Module Manufacturing Location	Manufacturing Code	--	
73-91	Module Part number	Module Part Number in ASCII	--	1
92-255	Reserved	Undefined	--	

Note 1:  
M2Y2G64TU8HD4B-BD → 4D325932473634545538484434422D42442020  
M2Y2G64TU8HD5B-BD → 4D325932473634545538484435422D42442020  
M2Y2G64TU8HD6B-BD → 4D325932473634545538484436422D42442020

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{IN}, V_{OUT}$	Voltage on I/O pins relative to $V_{SS}$	-0.5 to 2.3	V
$V_{DD}$	Voltage on VDD supply relative to $V_{SS}$	-1.0 to +2.3	V
$V_{DDQ}$	Voltage on VDDQ supply relative to $V_{SS}$	-0.5 to +2.3	V

**Note:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
$T_{OPER}$	Operating Temperature	0 to 85	°C	1, 2

- Operating Temperature is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95°C under all other specification parameters.
- Outside of this temperature range, even it is still within the limit of stress condition; some deviation on portion of operation specification may be required.
- Some application may require operating the DRAM up to 95°C case temperature. In this case above 85°C case temperature the Auto-Refresh command frequency has to be reduced to  $tREFI = 3.9\mu s$  and some AC timing parameter will reach or exceed their specified limit values.
- Self-Refresh period is hard-coded in the chip and therefore it is imperative that the system ensures the DRAM is below 85°C case temperature before initiating self-refresh operation.

## DC Electrical Characteristics and Operating Conditions

( $T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = 1.8V \pm 0.1V$ ;  $V_{DD} = 1.8V \pm 0.1V$ , See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
$V_{DD}$	Supply Voltage	1.7	1.9	V	1
$V_{DDQ}$	I/O Supply Voltage	1.7	1.9	V	1
$V_{SS}, V_{SSQ}$	Supply Voltage, I/O Supply Voltage	0	0	V	
$V_{REF}$	I/O Reference Voltage	$0.49V_{DDQ}$	$0.51V_{DDQ}$	V	1, 2
$V_{IH} (DC)$	Input High (Logic1) Voltage	$V_{REF} + 0.125$	$V_{DDQ} + 0.3$	V	1
$V_{IL} (DC)$	Input Low (Logic0) Voltage	-0.3	$V_{REF} - 0.125$	V	1

**Note:**

- Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- $V_{REF}$  is expected to be equal to 0.5  $V_{DDQ}$  of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on  $V_{REF}$  may not exceed 2% of the DC value.

## Environmental Parameters

Symbol	Parameter	Rating	Units	Note
$T_{OPR}$	Module Operating Temperature Range (ambient)	0 to 55	°C	3
$H_{OPR}$	Operating Humidity (relative)	10 to 90	%	
$T_{STG}$	Storage Temperature (Plastic)	-55 to 100	°C	1
$H_{STG}$	Storage Humidity (without condensation)	5 to 95	%	1
$P_{BAR}$	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

**Note:**

- Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Up to 9850 ft.
- The component maximum case temperature shall not exceed the value specified in the component spec.

## Operating, Standby, and Refresh Currents

T<sub>CASE</sub> = 0 °C ~ 85 °C; V<sub>DDQ</sub> = V<sub>DD</sub> = 1.8V ± 0.1V (1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-8500 (-BD)	Unit
I <sub>DD0</sub>	Operating Current: one bank; active/precharge; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1144	mA
I <sub>DD1</sub>	Operating Current: one bank; active/read/precharge; Burst = 2; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CL=2.5; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; address and control inputs changing once per clock cycle	1100	mA
I <sub>DD2P</sub>	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V <sub>IL</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN)	88	mA
I <sub>DD2N</sub>	Idle Standby Current: CS ≥ V <sub>IH</sub> (MIN); all banks idle; CKE ≥ V <sub>IH</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); address and control inputs changing once per clock cycle	792	mA
I <sub>DD2Q</sub>	Precharge Quiet Standby Current: All banks idle; $\overline{\text{CS}}$ is HIGH; CKE is HIGH; t <sub>CK</sub> = t <sub>CK</sub> (MIN); Other control and address inputs are stable, Data bus inputs are floating.	572	mA
I <sub>DD3PF</sub>	Active Power-Down Current: All banks open; t <sub>CK</sub> = t <sub>CK</sub> (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to <b>low</b> (Fast Power-down Exit).	440	mA
I <sub>DD3PS</sub>	Active Power-Down Current: All banks open; t <sub>CK</sub> = t <sub>CK</sub> (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to <b>high</b> (Slow Power-down Exit).	97	mA
I <sub>DD3N</sub>	Active Standby Current: one bank; active/precharge; CS ≥ V <sub>IH</sub> (MIN); CKE ≥ V <sub>IH</sub> (MIN); t <sub>RC</sub> = t <sub>RAS</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	660	mA
I <sub>DD4W</sub>	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t <sub>CK</sub> = t <sub>CK</sub> (MIN)	1232	mA
I <sub>DD4R</sub>	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA	1496	mA
I <sub>DD5</sub>	Auto-Refresh Current: t <sub>RC</sub> = t <sub>RFC</sub> (MIN)	2200	mA
I <sub>DD6</sub>	Self-Refresh Current: CKE ≤ 0.2V	97	mA
I <sub>DD7</sub>	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t <sub>RC</sub> = t <sub>RC</sub> (min); I <sub>OUT</sub> = 0mA.	2772	mA

**Note:** Module IDD was calculated from component IDD. It may differ from the actual measurement.

## Operating, Standby, and Refresh Currents

T<sub>CASE</sub> = 0 °C ~ 85 °C; V<sub>DDQ</sub> = V<sub>DD</sub> = 1.8V ± 0.1V (2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-8500 (-BD)	Unit
I <sub>DD0</sub>	Operating Current: one bank; active/precharge; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1804	mA
I <sub>DD1</sub>	Operating Current: one bank; active/read/precharge; Burst = 2; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CL=2.5; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; address and control inputs changing once per clock cycle	1760	mA
I <sub>DD2P</sub>	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V <sub>IL</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN)	176	mA
I <sub>DD2N</sub>	Idle Standby Current: CS ≥ V <sub>IH</sub> (MIN); all banks idle; CKE ≥ V <sub>IH</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); address and control inputs changing once per clock cycle	1584	mA
I <sub>DD2Q</sub>	Precharge Quiet Standby Current: All banks idle; $\overline{\text{CS}}$ is HIGH; CKE is HIGH; t <sub>CK</sub> = t <sub>CK</sub> (MIN); Other control and address inputs are stable, Data bus inputs are floating.	1144	mA
I <sub>DD3PF</sub>	Active Power-Down Current: All banks open; t <sub>CK</sub> = t <sub>CK</sub> (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to <b>low</b> (Fast Power-down Exit).	880	mA
I <sub>DD3PS</sub>	Active Power-Down Current: All banks open; t <sub>CK</sub> = t <sub>CK</sub> (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to <b>high</b> (Slow Power-down Exit).	194	mA
I <sub>DD3N</sub>	Active Standby Current: one bank; active/precharge; CS ≥ V <sub>IH</sub> (MIN); CKE ≥ V <sub>IH</sub> (MIN); t <sub>RC</sub> = t <sub>RAS</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1320	mA
I <sub>DD4W</sub>	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t <sub>CK</sub> = t <sub>CK</sub> (MIN)	1892	mA
I <sub>DD4R</sub>	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA	2156	mA
I <sub>DD5</sub>	Auto-Refresh Current: t <sub>RC</sub> = t <sub>RFC</sub> (MIN)	2860	mA
I <sub>DD6</sub>	Self-Refresh Current: CKE ≤ 0.2V	194	mA
I <sub>DD7</sub>	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t <sub>RC</sub> = t <sub>RC</sub> (min); I <sub>OUT</sub> = 0mA.	3432	mA

**Note:** Module IDD was calculated from component IDD. It may differ from the actual measurement.

## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T<sub>CASE</sub> = 0 °C ~ 85 °C; V<sub>DDQ</sub> = 1.8V ± 0.1V; V<sub>DD</sub> = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	PC2-8500		Unit
		Min	Max	
tCK	Clock Cycle Time (Average)	1875	8000	ps
tCH	CK high-level width (Average)	0.48	0.52	tCK
tCL	CK low-level width (Average)	0.48	0.52	tCK
WL	Write command to DQS associated clock edge	RL-1		nCK
tdQSS	Write command to 1st DQS latching transition	-0.25	0.25	tCK
tdSS	DQS falling edge to CK setup time(write cycle)	0.2	-	tCK
tdSH	DQS falling edge hold time from CK(write cycle)	0.2	-	tCK
tdQSL(H)	DQS input low (high) pulse width(write cycle)	0.35	-	tCK
tWPRE	Write preamble	0.35	-	tCK
tWPST	Write postamble	0.4	0.6	tCK
tIS	Address and control input setup time	125	-	ps
tIH	Address and control input hold time	200	-	ps
tIPW	Input pulse width	0.6	-	tCK
tdS	DQ and DM input setup time(differential data strobe)	0	-	ps
tdH	DQ and DM input hold time(differential data strobe)	75	-	ps
tdIPW	DQ and DM input pulse width (each input)	0.35	-	tCK
tAC	DQ output access time from CK/ $\overline{CK}$	-350	350	ps
tdQSK	DQS output access time from CK/ $\overline{CK}$	-350	350	ps
tHZ	Data-out high-impedance time from CK/ $\overline{CK}$	-	tAC max	ps
tLZ(DQS)	DQS low-impedance time from CK/ $\overline{CK}$	tAC min	tAC max	ps
tLZ(DQ)	DQ low-impedance time from CK/ $\overline{CK}$	2tAC min	tAC max	ps
tdQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	175	ps
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	Min(tCH(abs),tCL(abs))	-	ps
tQHS	Data hold Skew Factor	-	250	ps
tQH	Data output hold time from DQS	tHP - tQHS	-	ps
tRPRE	Read preamble	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	tCK
tRRD	Active bank A to Active bank B command	7.5	-	ns
tFAW	Four Activate Window for 1KB page size products	35	-	ns
tCCD	$\overline{CAS}$ to $\overline{CAS}$	2	-	nCK
tWR	Write recovery time without Auto-Precharge	15	-	ns
tdAL	Auto precharge write recovery + precharge time	WR + t <sub>nRP</sub>	-	nCK
tWTR	Internal write to read command delay	7.5	-	ns
tRTP	Internal read to precharge command delay	7.5	-	ns
tCKE	CKE minimum pulse width	3	-	nCK
tXSNR	Exit self refresh to a Non-read command	tRFC+10	-	ns
tXSRD	Exit self refresh to a Read command	200	-	nCK
tXP	Exit precharge power down to any Non- read command	3	-	nCK

## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

( $T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = 1.8\text{V} \pm 0.1\text{V}$ ;  $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ , See AC Characteristics) (Part 2 of 2)

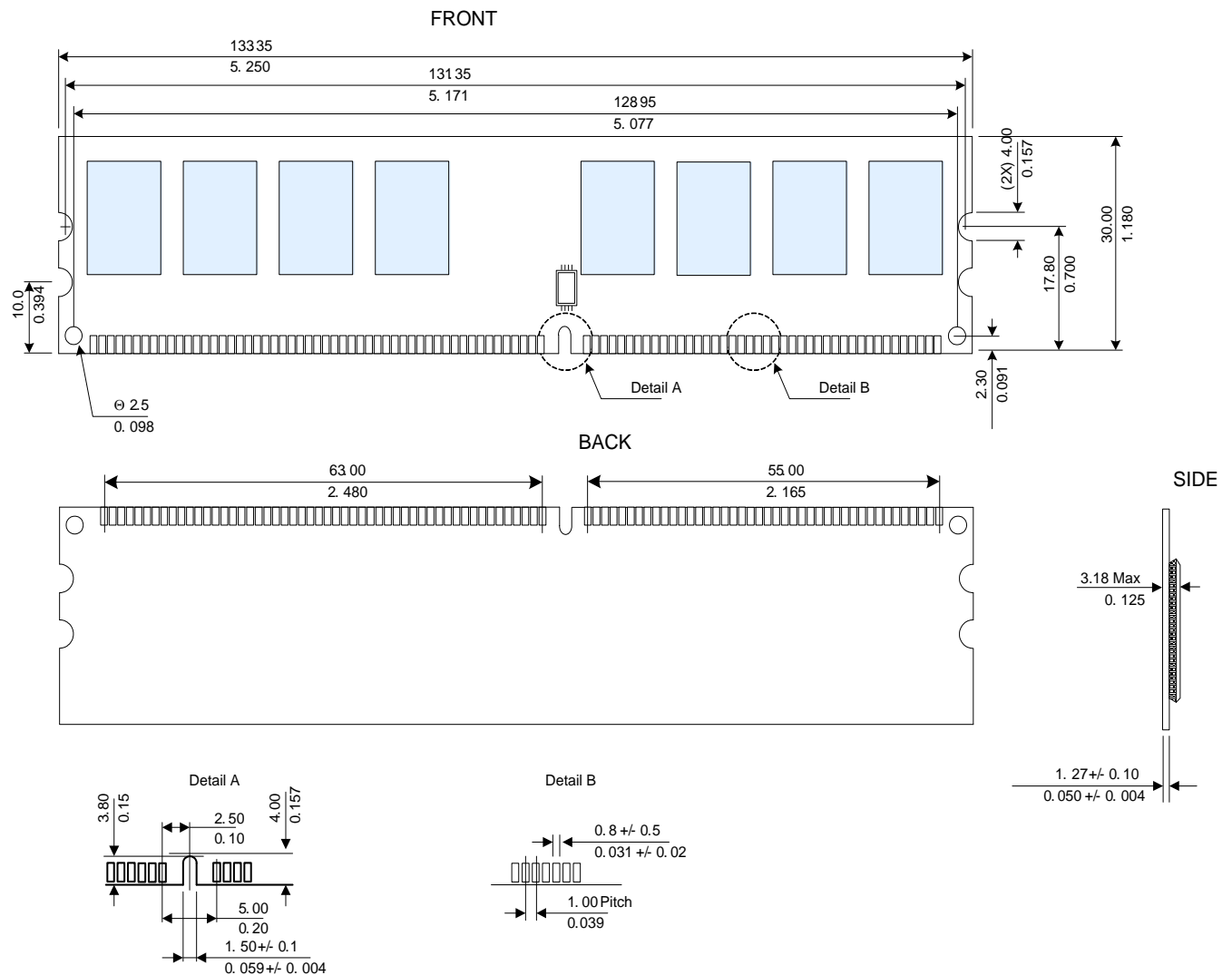
Symbol	Parameter	PC2-8500		Unit
		Min	Max	
tXARD	Exit active power down to read command	3	-	nCK
tXARDS	Exit active power down to read command	10 - AL	-	nCK
tAOND	ODT turn-on delay	2	2	nCK
tAON	ODT turn-on	tAC min	tAC max + 2.575	ns
tAONPD	ODT turn-on (Power down mode)	tAC min + 2	3tCK + tAC max + 1	ns
tAOFD	ODT turn-off delay	2.5	2.5	nCK
tAOF	ODT turn-off	tAC min	tAC max + 0.6	ns
tAOFPD	ODT turn-off (Power down mode)	tAC min + 2	2.5tCK+tAC max + 1	ns
tANPD	ODT to power down entry latency	4	-	nCK
tAXPD	ODT power down exit latency	11	-	nCK
tMRD	Mode register set command cycle time	2	-	nCK
tMOD	MRS command to ODT update delay	0	12	ns
tOIT	OCD drive mode output delay	0	12	ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	tIS + tCK + tIH	-	ns
tRFC	Refresh to active/Refresh command time	105	-	ns
tREFI	Average Periodic Refresh Interval ( $85^{\circ}\text{C} < T_{CASE} \leq 95^{\circ}\text{C}$ )	3.9	-	$\mu\text{s}$
	Average Periodic Refresh Interval ( $0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$ )	7.8	-	$\mu\text{s}$

## Speed Grade Definition

Symbol	Parameter	PC2-8500		Unit
		Min	Max	
tRAS	Row Active Time	45	70000	ns
tRC	Row Cycle Time	56.25	-	ns
tRCD	RAS to CAS delay	11.25	-	ns
tRP	Row Precharge Time	11.25	-	ns

## Package Dimensions

(1GB, 1Rank, 128Mx8 DDR2 SDRAMs)

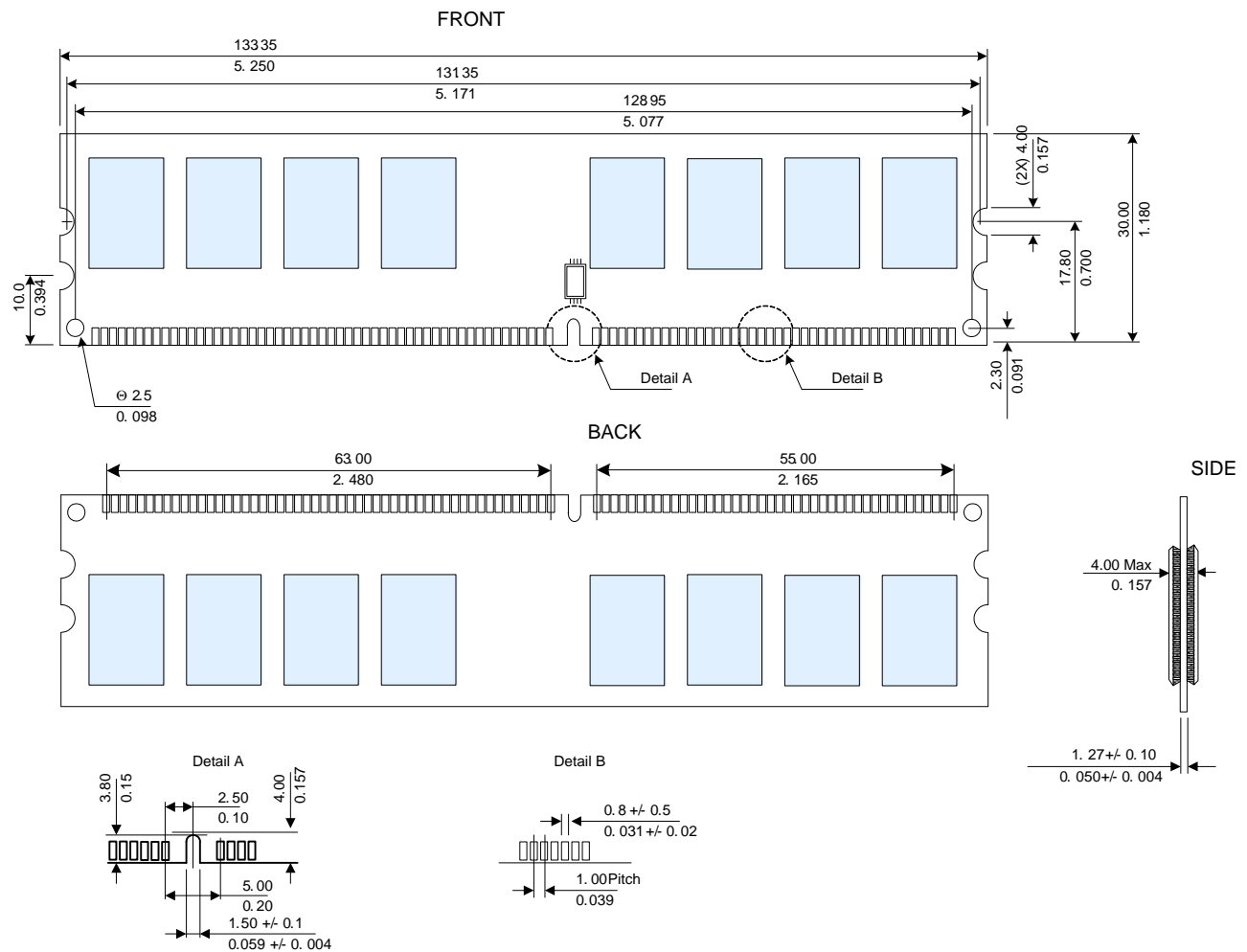


Note: All dimensions are typical with tolerances of  $\pm 0.15$  (0.006) unless otherwise stated

Units: Millimeters (Inches)

## Package Dimensions

(2GB, 2Ranks, 128Mx8 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of  $\pm 0.15$  (0.006) unless otherwise stated

Units: Millimeters (Inches)

M2Y1G64TU88D4B / M2Y2G64TU8HD4B / M2Y1G64TU88D5B / M2Y2G64TU8HD5B  
M2Y1G64TU88D6B / M2Y2G64TU8HD6B / M2Y1G64TU88D7B

1GB: 128M x 64 / 2GB: 256M x 64

Unbuffered DDR2 SDRAM DIMM



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## Revision Log

Rev	Date	Modification
0.1	04/2008	Preliminary Edition
1.0	07/2008	Official Release
1.1	10/2008	Add new part number