

240pin Unbuffered DDR2 SDRAM MODULE

Based on 128Mx8 DDR2 SDRAM D-die

Features

Performance:

		PC2-5300	PC2-6400	
Speed Sort		-3C	-AC	Unit
DIMM $\overline{\text{CAS}}$ Latency*		5	5	
f CK	Clock Frequency	333	400	MHz
t CK	Clock Cycle	3	2.5	ns
f DQ	DQ Burst Frequency	667	800	Mbps

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 128Mx64 and 256Mx64 DDR2 Unbuffered DIMM based on Elixir 128Mx8 DDR2 SDRAM D-die component
- Double Data Rate architecture; two data transfer per clock cycle
- Differential bi-directional data strobe (DQS & $\overline{\text{DQS}}$)
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK & $\overline{\text{CK}}$)
- Intended for 333MHz/400MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{\text{DD}} = V_{\text{DDQ}} = 1.8\text{V} \pm 0.1\text{V}$
- 7.8 μs Max. Average Periodic Refresh Interval
- Programmable Operation:
 - Device $\overline{\text{CAS}}$ Latency: 3, 4, 5
 - Burst Length: 4, 8
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/1 Addressing (row/column/rank) – 1GB
- 14/10/2 Addressing (row/column/rank) – 2GB
- Serial Presence Detect
- On Die Termination (ODT)
- OCD impedance adjustment.
- Gold contacts
- SDRAMs in 60-ball BGA Package
- RoHs Compliance.

Description

M2Y1G64TU88D0B, M2Y2G64TU8HD0B, M2Y1G64TU88D4B, M2Y2G64TU8HD4B, M2Y1G64TU88D5B, M2Y2G64TU8HD5B, M2Y1G64TU88D6B, M2Y2G64TU8HD6B and M2Y1G64TU88D7B are 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as one rank 128Mx64 and two ranks 256Mx64 high-speed memory array. M2Y1G64TU88D0B, M2Y1G64TU88D4B, M2Y1G64TU88D5B, M2Y1G64TU88D6B and M2Y1G64TU88D7B use eight 128Mx8 DDR2 SDRAMs and M2Y2G64TU8HD0B M2Y2G64TU8HD4B, M2Y2G64TU8HD5B and M2Y2G64TU8HD6B use sixteen 128Mx8 DDR2 SDRAMs in BGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All Elixir DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 333MHz (or 400MHz) clock speeds and achieves high-speed data transfer rates of up to 667Mbps (or 800Mbps). Prior to any access operation, the device $\overline{\text{CAS}}$ latency and burst / length /operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0, BA1 and BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

M2Y1G64TU88D0B / M2Y2G64TU8HD0B / M2Y1G64TU88D4B / M2Y2G64TU8HD4B
M2Y1G64TU88D5B / M2Y2G64TU8HD5B / M2Y1G64TU88D6B / M2Y2G64TU8HD6B
M2Y1G64TU88D7B



1GB: 128M x 64 / 2GB: 256M x 64

Unbuffered DDR2 SDRAM DIMM

Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M2Y1G64TU88D0B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300	128Mx64	GOLD	1.8V	
M2Y1G64TU88D0B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y1G64TU88D4B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300				
M2Y1G64TU88D4B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y1G64TU88D5B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300				
M2Y1G64TU88D5B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y1G64TU88D6B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300				
M2Y1G64TU88D6B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y1G64TU88D7B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y2G64TU8HD0B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300				
M2Y2G64TU8HD0B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y2G64TU8HD4B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300				
M2Y2G64TU8HD4B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y2G64TU8HD5B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300				
M2Y2G64TU8HD5B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				
M2Y2G64TU8HD6B-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300				
M2Y2G64TU8HD6B-AC	400MHz (2.50ns @ CL = 5)	DDR2-800	PC2-6400				

Pin Description

CK0~CK2 $\overline{\text{CK0}}\text{~}\overline{\text{CK2}}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS8	Bidirectional data strobes
$\overline{\text{RAS}}$	Row Address Strobe	DM0-DM8	Input Data Mask
$\overline{\text{CAS}}$	Column Address Strobe	$\overline{\text{DQS0}}\text{~}\overline{\text{DQS8}}$	Differential data strobes
$\overline{\text{WE}}$	Write Enable	VDD	Power (1.8V)
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	Chip Selects	VREF	Ref. Voltage for SSTL_18 inputs
A0-A9, A0-A13	Address Inputs	VDDSPD	Serial EEPROM positive power supply
A10/AP	Column Address Input/Auto-precharge	VSS	Ground
BA0 ~ BA2	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RESET	Reset pin	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	On-die termination control lines	SA0 ~ SA2	Serial Presence Detect Address Inputs
NC	No Connect		

Note: ODT1, CKE1 and $\overline{\text{CS1}}$ are only support in 2GB module type.

Pinout

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V _{REF}	42	NC	82	V _{SS}	121	V _{SS}	162	NC	202	DM4
2	V _{SS}	43	NC	83	$\overline{\text{DQS4}}$	122	DQ4	163	V _{SS}	203	NC
3	DQ0	44	V _{SS}	84	DQS4	123	DQ5	164	NC	204	V _{SS}
4	DQ1	45	NC ⁻	85	V _{SS}	124	V _{SS}	165	NC	205	DQ38
5	V _{SS}	46	NC	86	DQ34	125	DM0	166	V _{SS}	206	DQ39
6	$\overline{\text{DQS0}}$	47	V _{SS}	87	DQ35	126	NC	167	NC	207	V _{SS}
7	DQS0	48	NC	88	V _{SS}	127	V _{SS}	168	NC	208	DQ44
8	V _{SS}	49	NC	89	DQ40	128	DQ6	169	V _{SS}	209	DQ45
9	DQ2	50	V _{SS}	90	DQ41	129	DQ7	170	V _{DDQ}	210	V _{SS}
10	DQ3	51	V _{DDQ}	91	V _{SS}	130	V _{SS}	171	NC,CKE1	211	DM5
11	V _{SS}	52	CKE0	92	$\overline{\text{DQS5}}$	131	DQ12	172	V _{DD}	212	NC
12	DQ8	53	V _{DD}	93	DQS5	132	DQ13	173	NC	213	V _{SS}
13	DQ9	54	BA2	94	V _{SS}	133	V _{SS}	174	NC	214	DQ46
14	V _{SS}	55	NC	95	DQ42	134	DM1	175	V _{DDQ}	215	DQ47
15	$\overline{\text{DQS1}}$	56	V _{DDQ}	96	DQ43	135	NC	176	A12	216	V _{SS}
16	DQS1	57	A11	97	V _{SS}	136	V _{SS}	177	A9	217	DQ52
17	V _{SS}	58	A7	98	DQ48	137	CK1	178	V _{DD}	218	DQ53
18	NC	59	V _{DD}	99	DQ49	138	$\overline{\text{CK1}}$	179	A8	219	V _{SS}
19	NC	60	A5	100	V _{SS}	139	V _{SS}	180	A6	220	CK2
20	V _{SS}	61	A4	101	SA2	140	DQ14	181	V _{DDQ}	221	$\overline{\text{CK2}}$
21	DQ10	62	V _{DDQ}	102	NC	141	DQ15	182	A3	222	V _{SS}
22	DQ11	63	A2	103	V _{SS}	142	V _{SS}	183	A1	223	DM6
23	V _{SS}	64	V _{DD}	104	$\overline{\text{DQS6}}$	143	DQ20	184	V _{DD}	224	NC
24	DQ16		KEY	105	DQS6	144	DQ21		KEY	225	V _{SS}
25	DQ17	65	V _{SS}	106	V _{SS}	145	V _{SS}	185	CK0	226	DQ54
26	V _{SS}	66	V _{SS}	107	DQ50	146	DM2	186	$\overline{\text{CK0}}$	227	DQ55
27	$\overline{\text{DQS2}}$	67	V _{DD}	108	DQ51	147	NC	187	V _{DD}	228	V _{SS}
28	DQS2	68	NC	109	V _{SS}	148	V _{SS}	188	A0	229	DQ60
29	V _{SS}	69	V _{DD}	110	DQ56	149	DQ22	189	V _{DD}	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	V _{SS}
31	DQ19	71	BA0	112	V _{SS}	151	V _{SS}	191	V _{DDQ}	232	DM7
32	V _{SS}	72	V _{DDQ}	113	$\overline{\text{DQS7}}$	152	DQ28	192	$\overline{\text{RAS}}$	233	NC
33	DQ24	73	$\overline{\text{WE}}$	114	DQS7	153	DQ29	193	$\overline{\text{CS0}}$	234	V _{SS}
34	DQ25	74	$\overline{\text{CAS}}$	115	V _{SS}	154	V _{SS}	194	V _{DDQ}	235	DQ62
35	V _{SS}	75	V _{DDQ}	116	DQ58	155	DM3	195	ODT0	236	DQ63
36	$\overline{\text{DQS3}}$	76	NC, $\overline{\text{CS1}}$	117	DQ59	156	NC	196	A13	237	V _{SS}
37	DQS3	77	NC,ODT1	118	V _{SS}	157	V _{SS}	197	V _{DD}	238	V _{DDSPD}
38	V _{SS}	78	V _{DDQ}	119	SDA	158	DQ30	198	V _{SS}	239	SA0
39	DQ26	79	V _{SS}	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	V _{SS}	200	DQ37		
41	V _{SS}	81	DQ33			161	NC	201	V _{SS}		

Note:

1. NC = No Connect.
2. $\overline{\text{CS1}}$, ODT1 and CKE1 (Pins 76, 77 and 171) are only support in 2GB module type.

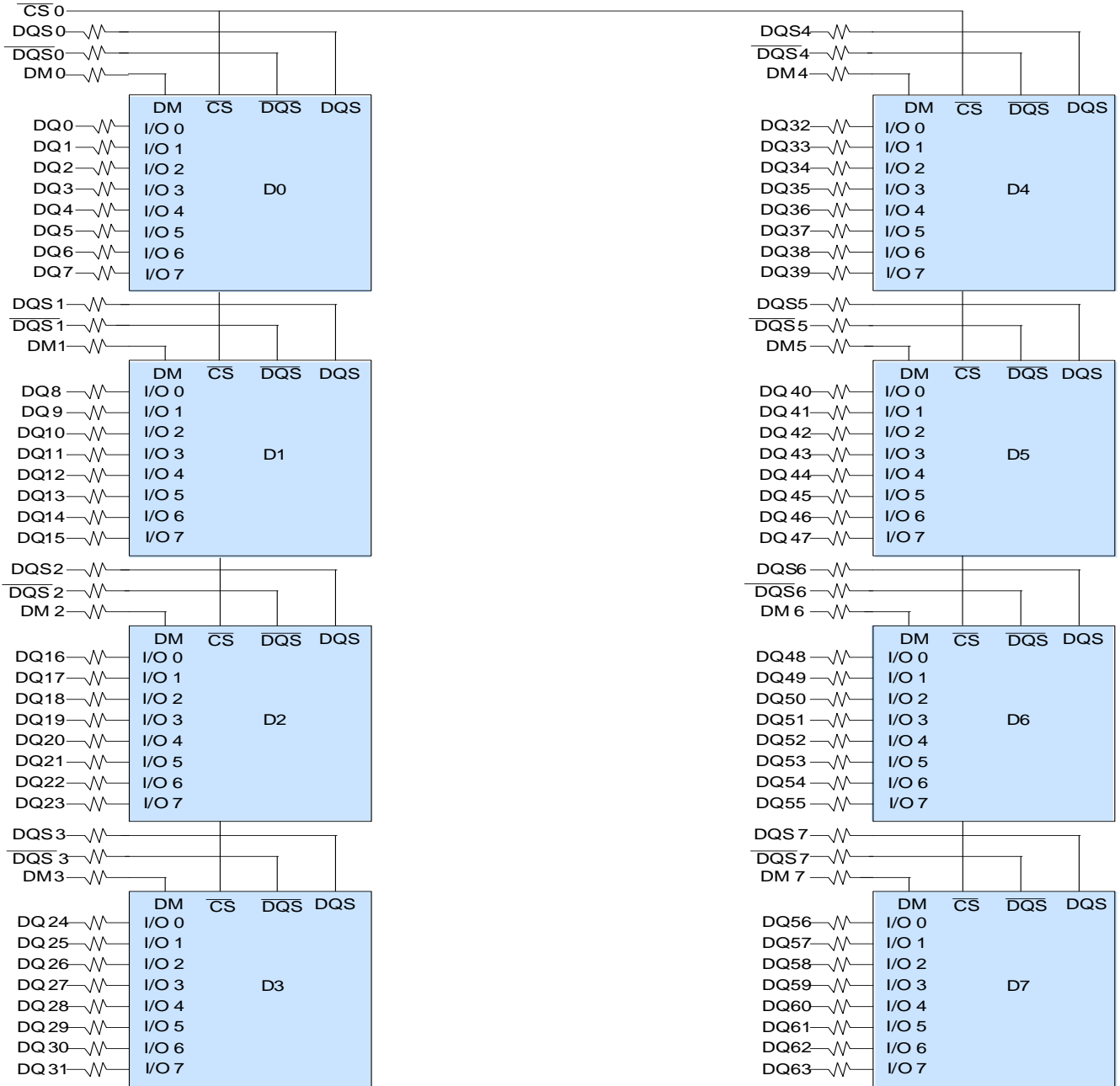
Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode. CKE1 apply on 2GB UDIMM only.
$\overline{CS0}$, $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. $\overline{CS1}$ apply on 2GB UDIMM only.
\overline{RAS} , \overline{CAS} , \overline{WE}	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, \overline{RAS} , \overline{CAS} , \overline{WE} define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL-18 inputs
VDDQ	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals. ODT1 apply on 2GB UDIMM only.
BA0 – BA2	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke "Autoprecharge" operation at the end of the Burst Read or Write cycle. If AP is high, Autoprecharge's selected and BA0/BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input /Output pins.
VDD, VSS	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic
DQS0 – DQS8 $\overline{DQS0}$ – $\overline{DQS8}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either VDD or VSS on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V DD to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V DD to act as a pull-up.
V DDSPD	Supply		Serial EEPROM positive power supply.

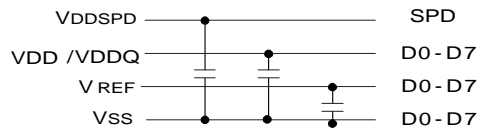
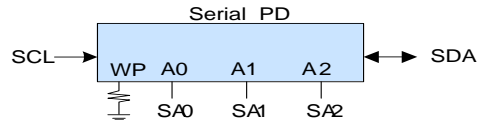
1GB: 128M x 64 / 2GB: 256M x 64

Unbuffered DDR2 SDRAM DIMM

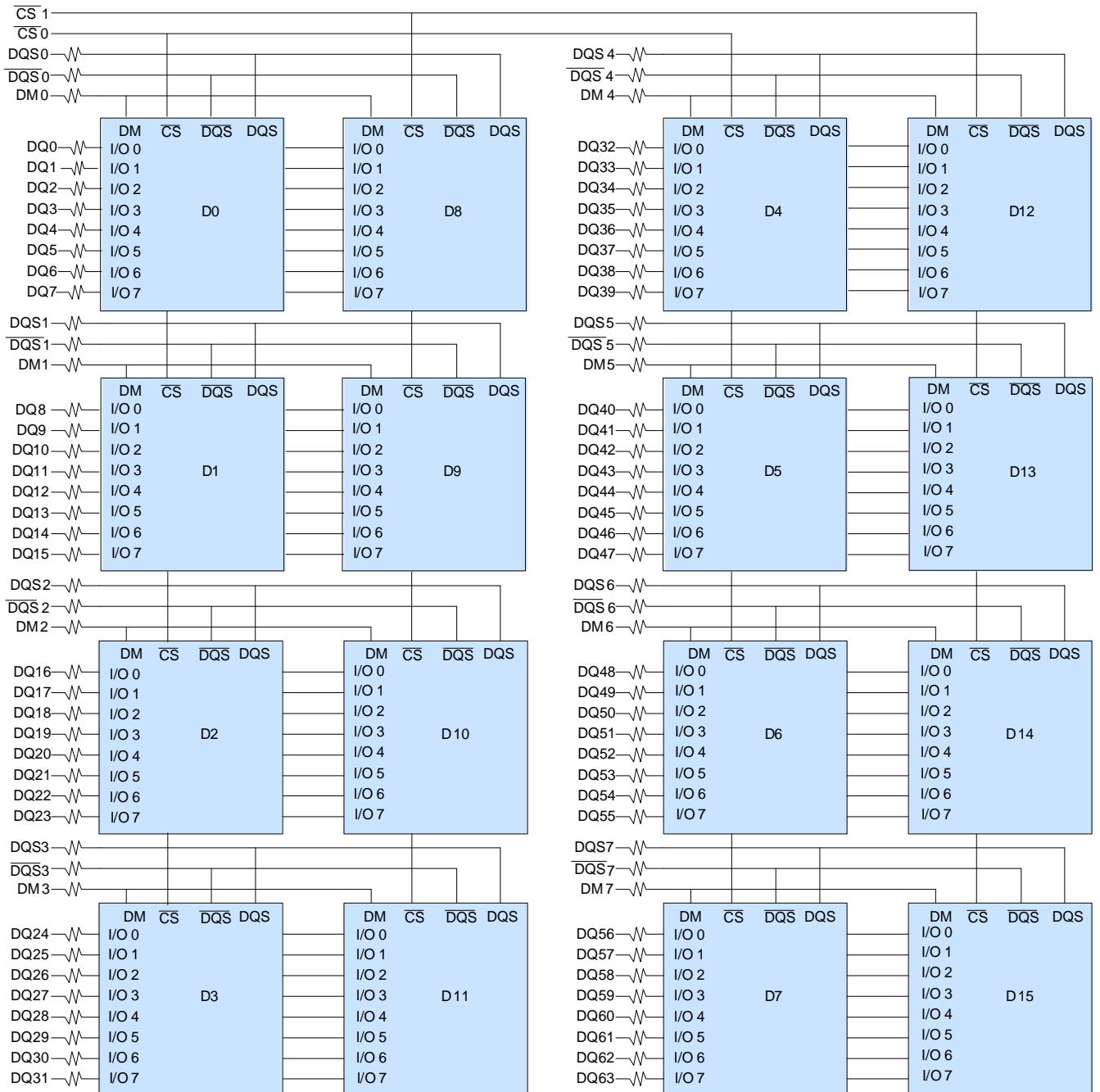
Functional Block Diagram (1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)



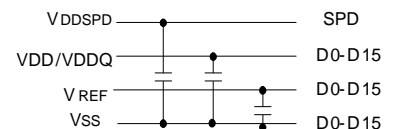
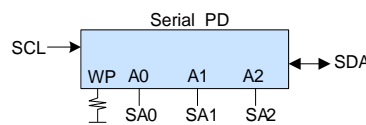
- BA0-BA2 → BA0-BA2: SDRAMs D0-D7
- A0-A13 → A0-A13: SDRAMs D0-D7
- RAS → RAS: SDRAMs D0-D7
- CAS → CAS: SDRAMs D0-D7
- WE → WE: SDRAMs D0-D7
- CKE0 → CKE: SDRAMs D0-D7
- ODT0 → ODT: SDRAMs D0-D7



Functional Block Diagram (2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)



- BA0-BA2 → BA0-BA2 : SDRAMs D0-D15
- A0-A13 → A0-A13 : SDRAMs D0-D15
- RAS → RAS : SDRAMs D0-D15
- CAS → CAS : SDRAMs D0-D15
- WE → WE : SDRAMs D0-D15
- CKE0 → CKE : SDRAMs D0-D7
- CKE1 → CKE : SDRAMs D8-D15
- ODT0 → ODT : SDRAMs D0-D7
- ODT1 → ODT : SDRAMs D8-D15



Serial Presence Detect -- Part 1 of 2 (1GB)

128Mx64 1 RANK UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		PC2-5300 -3C	PC2-6400 -AC	PC2-5300 -3C	PC2-6400 -AC	
0	Number of Serial PD Bytes Written during Production	128		80		
1	Total Number of Bytes in Serial PD device	256		08		
2	Fundamental Memory Type	DDR2		08		
3	Number of Row Addresses on Assembly	14		0E		
4	Number of Column Addresses on Assembly	10		0A		
5	Number of DIMM Ranks	1 rank, Height=30mm		60		
6	Data Width of Assembly	X64		40		
7	Reserved	Undefined		00		
8	Voltage Interface Level of this Assembly	SSTL_1.8V		05		
9	DDR2 SDRAM Device Cycle Time at CL=X	3ns	2.5ns	30	25	
10	DDR2 SDRAM Device Access Time from Clock at CL=X	0.45ns	0.4ns	45	40	
11	DIMM Configuration Type	Non parity/ECC		00		
12	Refresh Rate/Type	7.8μs		82		
13	Primary DDR2 SDRAM Width	X8		08		
14	Error Checking DDR2 SDRAM Device Width	Undefined		00		
15	Reserved	Undefined		00		
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8		0C		
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8		08		
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3,4,5		38		
19	DIMM Mechanical Characteristics	x ≤ 4.10 (mm)		01		
20	DDR2 SDRAM DIMM Type Information	UDIMM (133.35mm)		02		
21	DDR2 SDRAM Module Attributes:	Normal DIMM		00		
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50Ω ODT, and PASR		07		
23	Minimum Clock Cycle at CL=X-1	3.75ns		3D		
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns		50		
25	Minimum Clock Cycle Time at CL=X-2	5.0ns		50		
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns		60		
27	Minimum Row Precharge Time (t _{RP})	15ns	12.5ns	3C	32	
28	Minimum Row Active to Row Active delay (t _{RRD})	7.5ns		1E		
29	Minimum RAS to CAS delay (t _{RCD})	15ns	12.5ns	3C	32	
30	Minimum RAS Pulse Width (t _{RAS})	45ns		2D		
31	Module Bank Density	1GB		01		
32	Address and Command Setup Time Before Clock (t _{IS})	0.20ns	0.17ns	20	17	
33	Address and Command Hold Time After Clock (t _{IH})	0.27ns	0.25ns	27	25	
34	Data Input Setup Time Before Clock (t _{DS})	0.10ns	0.05ns	10	05	
35	Data Input Hold Time After Clock (t _{DH})	0.17ns	0.12ns	17	12	
36	Write Recovery Time (t _{WR})	15.0ns		3C		
37	Internal Write to Read Command delay (t _{WTR})	7.5ns		1E		
38	Internal Read to Precharge delay (t _{RTP})	7.5ns		1E		
39	Reserved	Undefined		00		

Serial Presence Detect -- Part 2 of 2 (1GB)

128Mx64 1 RANK UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		PC2-5300 -3C	PC2-6400 -AC	PC2-5300 -3C	PC2-6400 -AC	
40	Extension of Byte 41 t _{RC} and Byte 42 t _{RFC}	The number below a decimal point of t _{RC} and t _{RFC} are 0, t _{RFC} is less than 256ns.		06	36	
41	Minimum Core Cycle Time (t _{RC})	60.0ns	57.5ns	3C	39	
42	Min. Auto Refresh Command Cycle Time (t _{RFC})	127.5ns		7F		
43	Maximum Clock Cycle Time (t _{CK})	8.0ns		80		
44	Max. DQS-DQ Skew Factor (t _{DQS})	0.24ns	0.20ns	18	14	
45	Read Data Hold Skew Factor (t _{QHS})	0.34ns	0.30ns	22	1E	
46	PLL Relock Time	Undefined		00		
46-61	Reserved	Undefined		00		
62	SPD Revision	1.3		13		
63	Checksum for bytes 0-62	Checksum Data		17	FD	
64-71	Manufacture's JEDEC ID Code	NANYA		7F7F7F0B00000000		
72	Module Manufacturing Location	Manufacturing Code		--		
73-91	Module Part number	Module Part Number in ASCII		--		1
92-255	Reserved	Undefined		--		

Note 1:

M2Y1G64TU88D0B-3C → 4D325931473634545538384430422D33432020
M2Y1G64TU88D0B-AC → 4D325931473634545538384430422D41432020
M2Y1G64TU88D4B-3C → 4D325931473634545538384434422D33432020
M2Y1G64TU88D4B-AC → 4D325931473634545538384434422D41432020
M2Y1G64TU88D5B-3C → 4D325931473634545538384435422D33432020
M2Y1G64TU88D5B-AC → 4D325931473634545538384435422D41432020
M2Y1G64TU88D6B-3C → 4D325931473634545538384436422D33432020
M2Y1G64TU88D6B-AC → 4D325931473634545538384436422D41432020
M2Y1G64TU88D7B-AC → 4D325931473634545538384437422D41432020

Serial Presence Detect -- Part 1 of 2 (2GB)

256Mx64 2 RANKs UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		PC2-5300 -3C	PC2-6400 -AC	PC2-5300 -3C	PC2-6400 -AC	
0	Number of Serial PD Bytes Written during Production	128		80		
1	Total Number of Bytes in Serial PD device	256		08		
2	Fundamental Memory Type	DDR2		08		
3	Number of Row Addresses on Assembly	14		0E		
4	Number of Column Addresses on Assembly	10		0A		
5	Number of DIMM Ranks	2 ranks, Height=30mm		61		
6	Data Width of Assembly	X64		40		
7	Reserved	Undefined		00		
8	Voltage Interface Level of this Assembly	SSTL_1.8V		05		
9	DDR2 SDRAM Device Cycle Time at CL=X	3ns	2.5ns	30	25	
10	DDR2 SDRAM Device Access Time from Clock at CL=X	0.45ns	0.4ns	45	40	
11	DIMM Configuration Type	Non parity/ECC		00		
12	Refresh Rate/Type	7.8µs		82		
13	Primary DDR2 SDRAM Width	X8		08		
14	Error Checking DDR2 SDRAM Device Width	Undefined		00		
15	Reserved	Undefined		00		
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8		0C		
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8		08		
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3,4,5		38		
19	DIMM Mechanical Characteristics	x ≤ 4.10 (mm)		01		
20	DDR2 SDRAM DIMM Type Information	UDIMM (133.35mm)		02		
21	DDR2 SDRAM Module Attributes:	Normal DIMM		00		
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50Ω ODT, and PASR		07		
23	Minimum Clock Cycle at CL=X-1	3.75ns		3D		
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns		50		
25	Minimum Clock Cycle Time at CL=X-2	5.0ns		50		
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns		60		
27	Minimum Row Precharge Time (t _{RP})	15ns	12.5ns	3C	32	
28	Minimum Row Active to Row Active delay (t _{RRD})	7.5ns		1E		
29	Minimum RAS to CAS delay (t _{RCD})	15ns	12.5ns	3C	32	
30	Minimum RAS Pulse Width (t _{RAS})	45ns		2D		
31	Module Bank Density	1GB		01		
32	Address and Command Setup Time Before Clock (t _{IS})	0.20ns	0.17ns	20	17	
33	Address and Command Hold Time After Clock (t _{IH})	0.27ns	0.25ns	27	25	
34	Data Input Setup Time Before Clock (t _{DS})	0.10ns	0.05ns	10	05	
35	Data Input Hold Time After Clock (t _{DH})	0.17ns	0.12ns	17	12	
36	Write Recovery Time (t _{WR})	15.0ns		3C		
37	Internal Write to Read Command delay (t _{WTR})	7.5ns		1E		
38	Internal Read to Precharge delay (t _{RTP})	7.5ns		1E		
39	Reserved	Undefined		00		

M2Y1G64TU88D0B / M2Y2G64TU8HD0B / M2Y1G64TU88D4B / M2Y2G64TU8HD4B
M2Y1G64TU88D5B / M2Y2G64TU8HD5B / M2Y1G64TU88D6B / M2Y2G64TU8HD6B
M2Y1G64TU88D7B



1GB: 128M x 64 / 2GB: 256M x 64

Unbuffered DDR2 SDRAM DIMM

Serial Presence Detect -- Part 2 of 2 (2GB)

256Mx64 2 RANKs UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		PC2-5300 -3C	PC2-6400 -AC	PC2-5300 -3C	PC2-6400 -AC	
40	Extension of Byte 41 tRC and Byte 42 tRFC	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns.		06	36	
41	Minimum Core Cycle Time (tRC)	60.0ns	57.5ns	3C	39	
42	Min. Auto Refresh Command Cycle Time (tRFC)	127.5ns		7F		
43	Maximum Clock Cycle Time (tCK)	8.0ns		80		
44	Max. DQS-DQ Skew Factor (tQHS)	0.24ns	0.20ns	18	14	
45	Read Data Hold Skew Factor (tQHS)	0.34ns	0.30ns	22	1E	
46	PLL Relock Time	Undefined		00		
46-61	Reserved	Undefined		00		
62	SPD Revision	1.3		13		
63	Checksum for bytes 0-62	Checksum Data		18	FE	
64-71	Manufacturer's JEDEC ID Code	NANYA		7F7F7F0B00000000		
72	Module Manufacturing Location	Manufacturing Code		--		
73-91	Module Part number	Module Part Number in ASCII		--		1
92-255	Reserved	Undefined		--		

Note 1:

M2Y2G64TU8HD0B-3C → 4D325932473634545538484430422D33432020
M2Y2G64TU8HD0B-AC → 4D325932473634545538484430422D41432020
M2Y2G64TU8HD4B-3C → 4D325932473634545538484434422D33432020
M2Y2G64TU8HD4B-AC → 4D325932473634545538484434422D41432020
M2Y2G64TU8HD5B-3C → 4D325932473634545538484435422D33432020
M2Y2G64TU8HD5B-AC → 4D325932473634545538484435422D41432020
M2Y2G64TU8HD6B-3C → 4D325932473634545538484436422D33432020
M2Y2G64TU8HD6B-AC → 4D325932473634545538484436422D41432020

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5 to 2.3	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	-0.5 to 2.3	V
V_{DDQL}	Voltage on V_{DDQL} supply relative to V_{SS}	-0.5 to 2.3	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	-1.0 to +2.3	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Operating Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 95	°C	1,2,3
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	
I_L	Short Circuit Output Current	-5 to 5	Ma	

Note:

- Case temperature is measured at top and center side of any DRAMs.
- $t_{CASE} > 85^{\circ}C \rightarrow t_{REFI} = 3.9 \mu s$
- All DRAM specification only support $0^{\circ}C < t_{CASE} < 85^{\circ}C$

DC Electrical Characteristics and Operating Conditions

($T_{CASE} = 0^{\circ}C \sim 85^{\circ}C$; $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.7	1.9	V	1
V_{DDQ}	Supply Voltage for Output	1.7	1.9	V	1, 3
V_{DDL}	Supply Voltage for V_{DDQL}	1.7	1.9	V	3
V_{REF}	Input Reference Voltage	$0.49V_{DDQ}$	$0.51V_{DDQ}$	Mv	2
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	$V_{REF} + 0.04$	V	4
$V_{IH} (DC)$	Input High (Logic1) Voltage	$V_{REF} + 0.125$	$V_{DDQ} + 0.3$	V	
$V_{IL} (DC)$	Input Low (Logic0) Voltage	-0.3	$V_{REF} - 0.125$	V	

Note:

- Inputs are not recognized as valid until V_{REF} stabilizes.
- V_{REF} is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
- V_{DDQ} tracks with V_{DD} , V_{DDL} tracks with V_{DD} .
- V_{TT} of transmitting device track V_{REF} of receiving device.

Environmental Parameters

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Module Operating Temperature Range (ambient)	0 to 55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

Note:

- Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Up to 9850 ft.
- The component maximum case temperature shall not exceed the value specified in the component spec.

1GB: 128M x 64 / 2GB: 256M x 64

Unbuffered DDR2 SDRAM DIMM

Operating, Standby, and Refresh Currents

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ (1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-5300	PC2-6400	Unit
I _{DD0}	Operating Current: one bank; active/precharge; $T_{rc} = T_{rc}(\text{MIN})$; $T_{ck} = T_{ck}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	880	1012	Ma
I _{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; $T_{rc} = T_{rc}(\text{MIN})$; $CL=2.5$; $T_{ck} = T_{ck}(\text{MIN})$; $I_{OUT} = 0\text{Ma}$; address and control inputs changing once per clock cycle	792	924	Ma
I _{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL}(\text{MAX})$; $T_{ck} = T_{ck}(\text{MIN})$	88	88	Ma
I _{DD2N}	Idle Standby Current: $CS \geq V_{IH}(\text{MIN})$; all banks idle; $CKE \geq V_{IH}(\text{MIN})$; $T_{ck} = T_{ck}(\text{MIN})$; address and control inputs changing once per clock cycle	572	660	Ma
I _{DD2Q}	Precharge Quiet Standby Current: All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK}(\text{MIN})$; Other control and address inputs are stable, Data bus inputs are floating.	440	484	Ma
I _{DD3PF}	Active Power-Down Current: All banks open; $T_{ck} = T_{ck}(\text{MIN})$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to low (Fast Power-down Exit).	246	264	Ma
I _{DD3PS}	Active Power-Down Current: All banks open; $T_{ck} = T_{ck}(\text{MIN})$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to high (Slow Power-down Exit).	97	97	Ma
I _{DD3N}	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH}(\text{MIN})$; $CKE \geq V_{IH}(\text{MIN})$; $T_{rc} = T_{ras}(\text{MAX})$; $T_{ck} = T_{ck}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	528	616	Ma
I _{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL=2.5$; $T_{ck} = T_{ck}(\text{MIN})$	924	1056	Ma
I _{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 2.5$; $T_{ck} = T_{ck}(\text{MIN})$; $I_{OUT} = 0\text{Ma}$	1056	1188	Ma
I _{DD5}	Auto-Refresh Current: $T_{rc} = T_{rfc}(\text{MIN})$	1408	1540	Ma
I _{DD6}	Self-Refresh Current: $CKE \leq 0.2\text{V}$	97	97	Ma
I _{DD7}	Operating Current: four bank; four bank interleaving with $BL = 4$, address and control inputs randomly changing; 50% of data changing at every transfer; $T_{rc} = T_{rc}(\text{min})$; $I_{OUT} = 0\text{Ma}$.	1628	1804	Ma

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

1GB: 128M x 64 / 2GB: 256M x 64

Unbuffered DDR2 SDRAM DIMM

Operating, Standby, and Refresh Currents

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ (2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-5300	PC2-6400	Unit
I _{DD0}	Operating Current: one bank; active/precharge; $T_{rc} = T_{rc}(\text{MIN})$; $T_{ck} = T_{ck}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1408	1628	Ma
I _{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; $T_{rc} = T_{rc}(\text{MIN})$; $CL=2.5$; $T_{ck} = T_{ck}(\text{MIN})$; $I_{OUT} = 0\text{Ma}$; address and control inputs changing once per clock cycle	1320	1540	Ma
I _{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL}(\text{MAX})$; $T_{ck} = T_{ck}(\text{MIN})$	176	176	Ma
I _{DD2N}	Idle Standby Current: $CS \geq V_{IH}(\text{MIN})$; all banks idle; $CKE \geq V_{IH}(\text{MIN})$; $T_{ck} = T_{ck}(\text{MIN})$; address and control inputs changing once per clock cycle	1144	1320	Ma
I _{DD2Q}	Precharge Quiet Standby Current: All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK}(\text{MIN})$; Other control and address inputs are stable, Data bus inputs are floating.	880	968	Ma
I _{DD3PF}	Active Power-Down Current: All banks open; $T_{ck} = T_{ck}(\text{MIN})$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to low (Fast Power-down Exit).	493	528	Ma
I _{DD3PS}	Active Power-Down Current: All banks open; $T_{ck} = T_{ck}(\text{MIN})$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to high (Slow Power-down Exit).	194	194	Ma
I _{DD3N}	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH}(\text{MIN})$; $CKE \geq V_{IH}(\text{MIN})$; $T_{rc} = T_{ras}(\text{MAX})$; $T_{ck} = T_{ck}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1056	1232	Ma
I _{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL=2.5$; $T_{ck} = T_{ck}(\text{MIN})$	1452	1672	Ma
I _{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 2.5$; $T_{ck} = T_{ck}(\text{MIN})$; $I_{OUT} = 0\text{Ma}$	1584	1804	Ma
I _{DD5}	Auto-Refresh Current: $T_{rc} = T_{rfc}(\text{MIN})$	1936	2156	Ma
I _{DD6}	Self-Refresh Current: $CKE \leq 0.2\text{V}$	194	194	Ma
I _{DD7}	Operating Current: four bank; four bank interleaving with $BL = 4$, address and control inputs randomly changing; 50% of data changing at every transfer; $T_{rc} = T_{rc}(\text{min})$; $I_{OUT} = 0\text{Ma}$.	2156	2420	Ma

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	PC2-5300		PC2-6400		Unit
		Min.	Max.	Min.	Max.	
T _{ck}	Clock Cycle Time (Average)	3000	8000	2500	8000	ps
T _{ch}	CK high-level width (Average)	0.48	0.52	0.48	0.52	T _{ck}
T _{cl}	CK low-level width (Average)	0.48	0.52	0.48	0.52	T _{ck}
WL	Write command to DQS associated clock edge	RL-1		RL-1		Nck
T _{dqss}	Write command to 1 st DQS latching transition	-0.25	0.25	-0.25	0.25	T _{ck}
T _{dss}	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	T _{ck}
T _{dsh}	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	T _{ck}
T _{dqsl,(H)}	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	T _{ck}
T _{wpre}	Write preamble	0.35	-	0.35	-	T _{ck}
T _{wpst}	Write postamble	0.4	0.6	0.4	0.6	T _{ck}
T _{is}	Address and control input setup time	200	-	175	-	ps
T _{ih}	Address and control input hold time	275	-	250	-	ps
T _{ipw}	Input pulse width	0.6	-	0.6	-	T _{ck}
T _{ds}	DQ and DM input setup time (differential data strobe)	100	-	50	-	ps
T _{dh}	DQ and DM input hold time(differential data strobe)	175	-	125	-	ps
T _{dipw}	DQ and DM input pulse width (each input)	0.35	-	0.35	-	T _{ck}
T _{ac}	DQ output access time from CK/ $\overline{\text{CK}}$	-450	450	-400	400	ps
T _{dqack}	DQS output access time from CK/ $\overline{\text{CK}}$	-400	400	-350	350	ps
T _{hz}	Data-out high-impedance time from CK/ $\overline{\text{CK}}$	-	t _{AC} max	-	t _{AC} max	ps
T _{lz(DQS)}	DQS low-impedance time from CK/ $\overline{\text{CK}}$	t _{AC} min	t _{AC} max	t _{AC} min	t _{AC} max	ps
T _{lz(DQ)}	DQ low-impedance time from CK/ $\overline{\text{CK}}$	2t _{AC} min	t _{AC} max	2t _{AC} min	t _{AC} max	ps
T _{dqsq}	DQS-DQ skew (DQS & associated DQ signals)	-	240	-	200	ps
T _{hp}	Minimum half clk period for any given cycle; defined by clk high (T _{ch}) or clk low (T _{cl}) time	Min(T _{ch(ABS)} , T _{cl(ABS)})	-	Min(T _{ch(ABS)} , T _{cl(ABS)})	-	ps
T _{qhs}	Data hold Skew Factor	-	340	-	300	ps
T _{qh}	Data output hold time from DQS	t _{HP} – t _{QHS}	-	T _{HP} – T _{QHS}	-	ps
T _{rpre}	Read preamble	0.9	1.1	0.9	1.1	T _{ck}
T _{rpst}	Read postamble	0.4	0.6	0.4	0.6	T _{ck}
T _{rrd}	Active bank A to Active bank B command	7.5	-	7.5	-	ns
T _{faw}	Four Activate Window for 1KB page size products	37.5	-	35	-	ns
T _{ccd}	$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$	2	-	2	-	Nck
T _{wr}	Write recovery time without Auto-Precharge	15	-	15	-	ns
T _{dal}	Auto precharge write recovery + precharge time	WR+tnRP	-	WR+tnRP	-	Nck
T _{wtr}	Internal write to read command delay	7.5	-	7.5	-	ns
T _{trp}	Internal read to precharge command delay	7.5	-	7.5	-	ns
T _{cke}	CKE minimum pulse width	3	-	3	-	Nck
T _{xsnr}	Exit self refresh to a Non-read command	T _{rfc} +10	-	T _{rfc} +10	-	ns
T _{xsrd}	Exit self refresh to a Read command	200	-	200	-	Nck
T _{xp}	Exit precharge power down to any Non- read command	2	-	2	-	Nck

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

($T_{CASE} = 0^{\circ}C \sim 85^{\circ}C$; $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	PC2-5300		PC2-6400		Unit
		Min.	Max.	Min.	Max.	
T_{xard}	Exit active power down to read command	2	-	2	-	Nck
T_{xards}	Exit active power down to read command	7-AL		8-AL		Nck
T_{aond}	ODT turn-on delay	2	2	2	2	Nck
T_{aon}	ODT turn-on	$T_{ac}(\min)$	$T_{ac}(\max)+0.7$	$T_{ac}(\min)$	$T_{ac}(\max)+0.7$	ns
T_{aonpd}	ODT turn-on (Power down mode)	$T_{ac}(\min) + 2$	$2T_{ck} + T_{ac}(\max) + 1$	$T_{ac}(\min) + 2$	$2T_{ck} + T_{ac}(\max) + 1$	ns
T_{aofd}	ODT turn-off delay	2.5	2.5	2.5	2.5	Nck
T_{aof}	ODT turn-off	$T_{ac}(\min)$	$T_{ac}(\max) + 0.6$	$T_{ac}(\min)$	$T_{ac}(\max) + 0.6$	ns
T_{aofpd}	ODT turn-off (Power down mode)	$T_{ac}(\min)+2$	$2.5T_{ck} + T_{ac}(\max) + 1$	$T_{ac}(\min)+2$	$2.5T_{ck} + T_{ac}(\max) + 1$	ns
T_{anpd}	ODT to power down entry latency	3	-	3	-	Nck
T_{axpd}	ODT power down exit latency	8		8		Nck
T_{mrd}	Mode register set command cycle time	2	-	2	-	Nck
T_{mod}	MRS command to ODT update delay	0	12	0	12	ns
T_{oit}	OCD drive mode output delay	0	12	0	12	ns
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	$T_{is} + T_{ck} + T_{ih}$	-	$T_{is} + T_{ck} + T_{ih}$	-	ns
T_{rfc}	Refresh to active/Refresh command time	127.5		127.5		ns
T_{refi}	Average Periodic Refresh Interval ($85^{\circ}C < T_{CASE} \leq 95^{\circ}C$)	3.9		3.9		μs
	Average Periodic Refresh Interval ($0^{\circ}C \leq T_{CASE} \leq 85^{\circ}C$)	7.8		7.8		μs

Speed Grade Definition

Symbol	Parameter	PC2-5300		PC2-6400		Unit
		Min	Max	Min	Max	
T_{ras}	Row Active Time	45	70,000	45	70,000	ns
T_{rc}	Row Cycle Time	60	-	57.5	-	ns
T_{rzd}	RAS to CAS delay	15	-	12.5	-	ns
T_{rp}	Row Precharge Time	15	-	12.5	-	ns

M2Y1G64TU88D0B / M2Y2G64TU8HD0B / M2Y1G64TU88D4B / M2Y2G64TU8HD4B
M2Y1G64TU88D5B / M2Y2G64TU8HD5B / M2Y1G64TU88D6B / M2Y2G64TU8HD6B
M2Y1G64TU88D7B

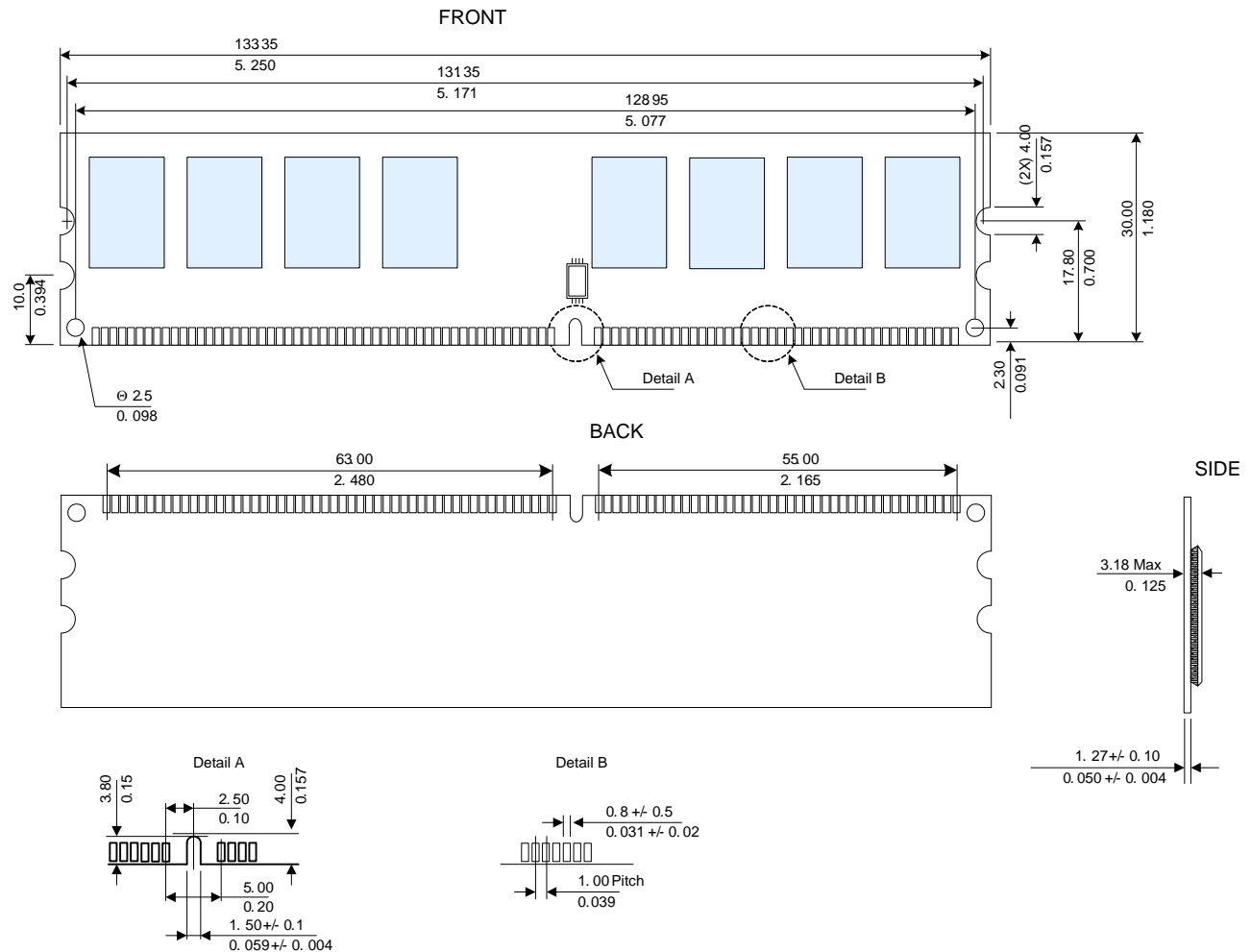


1GB: 128M x 64 / 2GB: 256M x 64

Unbuffered DDR2 SDRAM DIMM

Package Dimensions

(1GB, 1 Rank, 128Mx8 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated

Units: Millimeters (Inches)

M2Y1G64TU88D0B / M2Y2G64TU8HD0B / M2Y1G64TU88D4B / M2Y2G64TU8HD4B
M2Y1G64TU88D5B / M2Y2G64TU8HD5B / M2Y1G64TU88D6B / M2Y2G64TU8HD6B
M2Y1G64TU88D7B



1GB: 128M x 64 / 2GB: 256M x 64

Unbuffered DDR2 SDRAM DIMM

Revision Log

Rev	Date	Modification
0.1	03/2008	Preliminary Edition
1.0	04/2008	Official Release
1.1	07/2008	Revision update
1.2	10/2008	Add new part number